REMARKS

Claims 1-25 are currently pending in the present patent application. In the Office Action the Examiner allowed claims 12-25 and objected to claims 5 and 9-11, but indicated that claims 5 and 9-11 are allowable if appropriately rewritten in independent form. Claim 4 was also objected to due to a minor informality and this claim has been amended as the Examiner requested. The Examiner also rejected claims 1-4 and 6-8 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,384,318 to Hunter *et al.* ("Hunter").

Referring to Figure 2 of the present application, this figure is a functional block diagram of a detection and configuration circuit *200* for configuring a bidirectional buffer *202* in response to a signal applied on either a first node *204* or a second node *206* according to one embodiment of the present invention. *See* ¶18. One of the first node *204* or the second node *206* functions as the input of the buffer *202* and the other node functions as the output of the buffer. *Id.* The nodes 204 and 206 may be referred to as data nodes since the nodes function as data inputs or outputs once the buffer 202 has been configured. The function of each node depends on direction in which the buffer is configured to operate. *Id.* Note that these data nodes 204 and 206 also receive the configuration signals to configure the buffer 202. The detection and configuration circuit *200* configures the bidirectional buffer *202* responsive to signals applied on the input and output nodes *204*, *206* of the buffer and thus eliminates the need to route configuration lines to each buffer as with conventional bidirectional buffer circuits. *Id.* Conventional circuits require a significant number of physical lines be routed to provide the signals *108* to each of the memory cells *MC* and transfer the configuration data into the memory cells, as illustrated in Figure 1 of the present application. *See* ¶8. Such signals *108* may include reset, clocking, and data signals routed to the memory cells or even more physical lines for the signals perform required reset, addressing, and data transfer to the cells with associated complex configuration logic *106*.

Amended claim 1 recites a method of configuring a bidirectional buffer including first and second data signal nodes. The method includes applying a configuration signal on one of the first and second data signal nodes and configuring the buffer responsive to the applied configuration signal. Claim 1 now expressly recites that the configuration signal which configures the bidirectional buffer is applied on one of the data signal nodes of the buffer. Thus, no separate configuration signal lines need be run to each buffer.

In contrast, the Hunter patent discloses as shown in Figure 3 a conventional configuration approach including data lines in N-bit data busses 110-1 and 110-2 coupled to a bidirectional buffer 320. Separate indicator lines INDICATOR A and INDICATOR B are applied to a direction control block 310 associated with the buffer 320 to program the direction of the buffer. *See*, col. 3, lines 58-62. With Hunter the configuration signals to set the direction of operation of the buffers 320 are not applied to the data inputs or busses 110-1 or 110-2 of the buffer 320, but instead are applied on the separate configuration lines INDICATOR A and INDICATOR B. Therefore, Hunter neither discloses nor suggests applying a configuration signal on one of the first and second data signal nodes of the bidirectional buffer and configuring the buffer responsive to the applied configuration signal. Instead, in Hunter the configuration signals are applied on signal lines separate from the data lines of the buffer.

For these reasons, Hunter neither discloses nor suggests the method recited in amended claim 1 and this claim is therefore allowable. Independent claim 8 has been amended similar to claim 1 to expressly recite that the configuration signal is applied to one of a first and second data signal node and is allowable for reasons similar to those just discussed with regard to claim 1. The amendments to claims 1 and 8 do not narrow the scopes of these claims but merely utilize alternate terminology for the recited nodes to more clearly convey that these nodes to which the configuration signals are applied are the data nodes of the recited bidirectional buffers.

The Examiner also made of record U.S. Patent Nos. 5,923,187 to Maugars ("Maugars") and 5,214,330 to Okazaki ("Okazaki"). With regard to amended claim 8, neither of these references discloses "storing a first memory bit

responsive to the applied configuration signal" and "enabling the buffer to operate in a first direction responsive to the stored memory bit." With regard to claim 1, neither reference discloses "configuring the buffer responsive to the applied configuration signal." Instead, in Okazaki and Maugars each buffer operates in both directions responsive to applied data signals and not configuration signals. The combinations of elements recited in amended claims 1 and 8 are therefore also allowable over Maugars and Okazaki.

The claims dependent on the independent claims are allowable for the same reasons as the independent claims, and because of the additional limitations added by the dependent claims. Specifically, claims 5 and 9-11, which were objected to by the Examiner but indicated as allowable if appropriately rewritten in independent form, have not been rewritten but are allowable due to amended claims 1 and 8 from which they depend being allowable.

The above discussion of the embodiment of Figure 2 and the subsequent comparison of this embodiment to the Hunter patent should not be construed to define the scope or interpretation of any of the claims. This disclosed embodiment of the invention was discussed in comparison to the applied Hunter patent merely to help the Examiner appreciate certain distinctions between the pending claims and the subject matter of the Hunter patent.

Enclosed herewith is a change of Correspondence Address Form. Please note, as indicated on the Declaration, all PTO Correspondence for this application is to be mailed to:

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The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to resolve the matter. If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application,

kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

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